

Notice of References Cited	Application/Control No. 10/038,209	Applicant(s)/Patent Under Reexamination RICH ET AL.	
	Examiner A. M. Thompson	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2003/0125918	07-2003	Rich et al.	703/14
	B	US-5,875,111	02-1999	Patel	703/19
	C	US-2003/0125917	07-2003	Rich et al.	703/14
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Fleischmann et al., OLIVIA: Objectoriented Logicsimulation Implementing the VITAL Standard, Proceedings of the Seventh Great Lakes Symposium on VLSI, pages 51-56, March 1997.
	V	Balaji et al, Modeling ASIC Memories in VHDL, Proceedings of the Conference with EURO-VHDL '96 and Exhibition on European Design Automation, pages 502-508, September 1996.
	W	S. Krolikoski, Standardizing ASIC Libraries in VHDL Using VITAL: A Tutorial, IEEE 1995 Custom Integrated Circuits Conference, pages 603-610, May 1995.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.